A measurement technique for circumventing hysteresis and conductance drift in carbon nanotube field-effect transistors

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Abstract

We present a measurement protocol that effectively eliminates both the hysteresis and the temporal drift typically observed in the channel conductance of single-walled carbon nanotube field-effect transistors (SWNT FETs) during the application of gate voltages. Before each resistance measurement, the gate is first stepped through a series of alternating positive and negative voltages to produce a neutral charge distribution within the device. This process is highly effective at removing the hysteresis in the channel conductance, and time-dependent measurements further demonstrate that the drain current is stable and single-valued, independent of the prior measurement history. The effectiveness of this method can be understood within the Preisach hysteresis model, which we demonstrate as a useful framework to predict the observed results.

Keywords: carbon nanotubes, hysteresis, Preisach

(Some figures may appear in colour only in the online journal)

1. Introduction

The unique electronic properties of single-walled carbon nanotubes (SWNTs) make them valid candidates for a wide variety of applications, including memory devices [1–3] and sensors of chemical [4–6], biochemical [7–9], and electromechanical [10–12] stimuli. The diversity of their potential applications is largely due to the fact that electronic conduction in SWNTs is heavily influenced by the chemical and electrostatic environment. However, this sensitivity can also cause current instability and significant hysteresis in the gate voltage response of a field-effect transistor (FET), both of which are often attributed to charge traps in the dielectric and substrate [1, 13–17]. Charge trap states can bias the gate potential, changing the channel conductance in undesirable ways and complicating the extraction of device parameters, such as mobility. Furthermore, if SWNTs are to be integrated into practical circuits, the drain current at a given gate voltage should be stable and reproducible.

The charge trap states in the gate dielectric can comprise a mixture of both acceptor and donor states existing within the mobility gap of the gate dielectric, in addition to other possible mid-gap states [18]. The density and occupancy properties of these charge traps will in general depend on the composition and fabrication process for the dielectric material. A standard approach to mitigating these issues involves improving the quality of the dielectric through careful attention to chemical purity and processing history, but even the best fabrication techniques still produce charge trap densities that influence...
the performance of SWNT FETs. It has been recognized that charge can be mobile among the trap states and this can produce a time-dependent response as the trapped charge gradually equilibrates back to a neutralized state. On this basis, a measurement protocol has been proposed that involves waiting for equilibration between short voltage pulses to the gate electrode [19]. An additional approach has been proposed that alternates between positive and negative gate voltages for each measurement, in an effort to mitigate the resulting hysteresis in the source–drain current [20, 21]. As we show below, both of these approaches, while providing substantial benefits, still leave undesirable artifacts. Previous work has shown that triangular ambipolar pulses can be used to initialize nanotube devices prior to probing the threshold voltage [22]. The results presented here are in general agreement with the results presented in [22], but here we will show and confirm with the Preisach model that the device hysteresis can be effectively removed with half of the waveform reported in [22].

We propose a measurement technique that overcomes these effects of charge trap states for SWNT FETs, allowing the measurement of non-hysteretic transfer curves and reproducible drain current values, even when the FETs themselves show history-dependence in conventional measurements. The technique is analogous to magnetic degaussing, where hysteresis in the magnetic response of metals is overcome by using alternating positive and negative magnetic fields that gradually decrease in amplitude to produce a de-magnetized state [23]. Our proposed measurement protocol calls for the successive reversal of the gate potential around a desired point of charge neutrality, typically zero applied gate voltage. A schematic waveform is shown in figure 1(a), where the gate voltage is stepped through a series of alternating positive and negative values of decreasing amplitude between the desired measurements, which are indicated by the triangles labeled 1, 2, and 3. The oscillations performed between the short pulsed measurements (1, 2, 3) set a quasi-neutral charge distribution in the SWNT FET, eliminating the effects of the previous measurement pulse, thus allowing the pulsed measurements to be effectively independent of each other. Below we compare this new measurement protocol to two others introduced above [19–21], and we show that the process is highly effective at removing both the hysteresis and the drift in the channel conductance, effectively producing a neutral charge configuration in the dielectric. We model the observations using the framework proposed by Preisach and show that by appropriate choice of waveform parameters, such as gate voltage step size, the hysteresis effects can be made arbitrarily small within the model.

2. Experimental details

To demonstrate the protocol, we fabricate a set of SWNT FETs from parallel nanotubes grown on quartz substrates following published chemical vapor deposition procedures [24, 25]. A schematic diagram of the device design is shown in figure 1(b), where approximately 200 aligned SWNTs on quartz are contacted by source and drain electrodes and then encapsulated in 65 nm of an Al\textsubscript{2}O\textsubscript{3} dielectric layer, which is then subsequently covered with a gold top-gate electrode. The channel width and length were 100 \(\mu\)m and 10 \(\mu\)m, respectively, and used an 8 \(\mu\)m wide gate. The source, drain, and gate electrodes were composed of 50 nm of gold, with a 5 nm titanium adhesion layer.

The typical behavior of such an FET is shown in figure 1(c), which shows the drain current versus gate voltage of a typical device, exhibiting a large hysteresis as the difference in drain current recorded during increasing and decreasing applied gate potential. One method to quantify the hysteresis is to track horizontal shifts in data plotted as in figure 1(c) by defining a threshold voltage, \(V_{th}\), as a function of gate voltage, \(V_{gs}\), at a constant source–drain voltage of 5 V, for the SWNT FET structure shown in figure 1(b). The hysteresis of this curve is visible as the drain current difference between the positive and negative gate voltage sweeps.

Figure 1. (a) Gate voltage waveform used to acquire hysteresis-free transfer curves. The drain current is only measured at the black triangles (1, 2, 3). (b) Schematic and circuit diagram of an SWNT FET with SWNTs encapsulated in Al\textsubscript{2}O\textsubscript{3}. The side inset shows a scanning electron microscope image of the nanotubes in the channel, with a channel length \(L = 10 \mu m\). (c) Drain current, \(I_d\), as a function of gate voltage, \(V_{gs}\), at a constant source–drain voltage of 5 V, for the SWNT FET structure shown in figure 1(b). The hysteresis of this curve is visible as the drain current difference between the positive and negative gate voltage sweeps.
3. Drift of drain current

In addition to the hysteresis, another way to observe the influence of trapped charge on device performance is to observe the time dependence, or drift, of the SWNT FET drain current after a change in gate voltage. If there is no change in the occupation of charge trap states, the drain current will remain constant at a fixed gate bias. If change in the occupation of charge trap states occurs, the drain current will approach an equilibrium value as the trapped charge distribution equilibrates over time, with a time constant determined by the mobility of the trapped charge. To quantify the drain current time dependence, we present results with the following measurement technique. First, the gate dielectric is allowed to relax to an equilibrium state by holding the applied gate potential at $V_{gs} = 0$ V for at least 1000 s. Once the drain current drift is less than 1 µA per 100 s (at applied source–drain bias of $V_{sd} = 5$ V), measurements are initiated. A gate voltage pulse of magnitude $V_{gs\ pulse}$ and duration $T_{on}$ is applied to temporarily draw charge into the gate dielectric. The gate is then returned to $V_{gs} = 0$ V and the drain current is measured for 100 s as the dielectric re-equilibrates. The gate is then returned to $V_{gs} = 0$ V and the drain current is measured for 100 s as the dielectric re-equilibrates. Next, a gate voltage pulse of the same magnitude and duration but with opposite polarity ($-V_{gs\ pulse}$) is applied, and after returning the gate to $V_{gs} = 0$ V, the drain current is again measured for 100 s. Pulse generation and data acquisition were performed with a Keithley 2612A source-meter, with a voltage sourcing resolution of 1 µs and current measuring resolution of 5 nA. Two sets of measurements investigating the dependence on both parameters, $V_{gs\ pulse}$ and $T_{on}$, were performed, and the results are summarized in figure 2.

In the first measurement set, $T_{on} = 1$ ms and $V_{gs\ pulse}$ increases from 1 to 10 V in steps of 1 V (see inset of figure 2(a)). In the second measurement set, $V_{gs\ pulse} = 1$ V and $T_{on}$ increases from 1 ms to 1000 s by three points per decade (see inset of figure 2(b)). The rate of change of the drain current was greatest immediately after the gate voltage pulse and slowed with time, usually with most of the change occurring in the first second. To better capture this behavior, the time axes in figures 2(a) and (b) are plotted on a logarithmic scale. The equilibrium current subtracted from the drain current is plotted along the vertical axis. For these measurements, the equilibrium current was near 420 µA (divided amongst the ~200 SWNTs in the channel). The same measurements were performed on several other SWNT FETs with similar results.

As expected, the trend for increasing $V_{gs\ pulse}$ and $T_{on}$ values results in longer times to reach equilibrium. The drain current follows a roughly linear or even super-linear dependence on the logarithm of time, making it difficult to
quantify exactly when the drain current reaches equilibrium. For the largest values of $V_{gs\text{ Pulse}}$ and $T_{on}$, the current not only fails to reach equilibrium in 100 s but by projecting the trends forward appears to require several orders of magnitude more time, which presents experimental challenges for obtaining measurements at the equilibrium state. Due to these challenges, the time-dependent results are better quantified by the initial current difference from equilibrium, rather than the equilibration time. Due to the time resolution of the measurements, the current 1 ms after the gate voltage pulse is considered to be the initial current, shown as a dashed box in figures 2(a) and (b) and plotted in figures 2(c) and (d). This $I_D$ value has a slightly super-linear dependence on $V_{gs\text{ Pulse}}$ and a roughly linear dependence on the logarithm of $T_{on}$.

These data provide two lessons useful for designing a measurement technique for restoring a gated conduction channel to a low energy charge configuration. First, to minimize the amount of charge trapped during a non-zero gate voltage measurement, pulses of minimal duration should be used both in making the measurements and in the restoring waveform. With the measurement equipment used for these studies, each pulse can be approximately 1 ms. Second, considering common input voltages in the range of ±10 V and typical measurement times below 100 s, the gate voltage magnitude has a larger impact on trap occupation than does its duration. This indicates that a method of using the gate voltage to actively force the charges into a neutralized state would not only be faster than merely waiting for the traps to reach equilibrium but would also be more effective. Our data show that even with our minimum pulse duration ($T_{on} = 1$ ms), the drain current after a gate pulse of 10 V will not reach equilibrium for times longer than 100 s, by orders of magnitude, an undesirable amount of time for characterizing electronic devices. If the trapped charge could be neutralized by the application of an appropriate sequence of applied voltages, the drain current should be forced into equilibrium and the time dependence should disappear. We will demonstrate this later in section 4.

4. Comparisons of measurement waveforms

In this section, the effectiveness of specific measurement waveforms will first be evaluated by the hysteresis of a transfer curve and then we will investigate the time dependence of the drain current after each measurement. Other strategies have also recently been published to reduce hysteresis in the transfer curves of SWNT FETs [19–22]. Here, we compare two strategies together with our own proposed strategy, showing that our degaussing-inspired approach is quite effective at producing a reproducible transistor response within a reasonable amount of measurement time.

The four gate voltage waveforms being evaluated are shown in figure 3, labeled A–D. The first waveform (A) is a conventional transfer curve measurement, a linear sweep of the gate potential. The second waveform (B) uses short 1 ms gate voltage pulses to measure drain current, with an additional 10 s hold at ground between each measurement pulse to allow trapped charge to relax [19]. The third waveform (C) also uses 1 ms gate voltage pulses, of alternating polarity, with $V_{gs} = 0$ for 1 ms between the pulses. The rationale for this waveform is to quickly neutralize injected charge by the immediate subsequent injection of charge of the opposite sign [20–22]. The last waveform (D) incorporates our approach of using a full restoring waveform to return the gate dielectric to a neutral charge configuration after each measurement. In waveform D, $V_{gs}$ pulses of 1 ms are used with a series of alternating pulses, decreasing in magnitude, executed after each measurement pulse. During this restoring waveform, the gate potential oscillates through $N$ linearly decreasing positive/negative cycles, with $N = 100$ chosen for demonstration purposes here. Transfer curves using all four measurement waveforms are shown in figure 3. Each was taken on the same SWNT FET with the gate voltage swept between ±10 V in steps of 100 mV with a constant source–drain bias of 5 V. To clearly see each transfer curve, they are offset from each other along the horizontal axis by 10 V.

The threshold voltages for both the forward and reverse sweeps are extracted by the linear extrapolation method at the point of maximum transconductance [26]. The regression coefficients for the fits range from $r = 0.99649$ to 0.99965, indicating good fits to the data. The threshold voltages listed in table 1 are an average of the forward and reverse values with their corresponding uncertainty range. As mentioned above, the hysteresis width, $\Delta V_{th}$, is the difference in forward and reverse threshold voltages. The acquisition time is the length of time required to take the full transfer curve. These three parameters are listed in table 1. As expected, waveform A executes the fastest, taking less than one second with our measurement setup, but produces the greatest amount of hysteresis. This transfer curve is considered the control to which the others will be compared. Waveform B reduces
ΔVth by a factor of 4.0, but the 10 s pause between each measurement pulse causes the full transfer curve to take over an hour to acquire. Waveform C reduces ΔVth by a factor of 23, and only takes twice as long as waveform A to acquire. Our waveform, D, brings ΔVth down to the level of our measurement noise, more than 150 times smaller than the original level. The extra voltage pulses from executing the restoring waveform after each measurement pulse extend the acquisition time to just under 30 s, a reasonable time frame for acquiring a full and accurate transfer curve. We note that the threshold voltage is sensitive to changes in both the transconductance and the zero gate bias drain current, and that analysis of figure 3 reveals that the difference in forward and backward transconductance decreases significantly from method A to method D. Consequently, the uncertainty in the extracted threshold voltage also decreases from method A to D, while the difference in the forward and backward zero gate bias drain decreases significantly from method A to method D. Clearly, waveform D reduces the hysteresis far beyond the other measurement techniques tested here, effectively eliminating it within the accuracy of our measurements.

Now we turn our attention to the stability of the drain current and the effectiveness of the different measurement protocols for removing drift. If the charge injected into the dielectric has been successfully forced into a stable neutralized configuration, the drain current should remain stable, rather than drifting toward an equilibrium value as was shown in figure 2. Figure 4 shows the drain current for 100 s after executing the restoring waveform after 1 ms gate voltage pulses of +9 and −9 V without a restoring waveform (black) and with a restoring waveform (green). Diagrams of the measurement waveforms are shown as insets. The green data points show no measurable time dependence and only negligible static offset.

### Table 1. Hysteresis data (ΔVth and Vth) from the Ieq versus Vgs data in figure 3. The hysteresis width (ΔVth) decreases from method A to D, while the uncertainty in the extracted threshold voltage also decreases from method A to D.

<table>
<thead>
<tr>
<th>Method</th>
<th>ΔVth (V)</th>
<th>Vth (V)</th>
<th>Acquisition time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.8</td>
<td>5.04 ± 18%</td>
<td>0.925</td>
</tr>
<tr>
<td>B</td>
<td>0.44</td>
<td>3.25 ± 6.8%</td>
<td>4013</td>
</tr>
<tr>
<td>C</td>
<td>0.08</td>
<td>3.53 ± 2.5%</td>
<td>1.90</td>
</tr>
<tr>
<td>D</td>
<td>0.01</td>
<td>3.95 ± 0.32%</td>
<td>29.4</td>
</tr>
</tbody>
</table>

5. **Preisach hysteresis model**

While the measurement protocol we present above is relatively straightforward to implement and evaluate, it would nevertheless be useful to develop a theoretical framework to predict its performance and to compare against possible further improved protocols in the future. In general, charge traps come in a variety of types [27, 28], including electron traps that may switch between neutral and negatively charged states, hole traps that may switch between neutral and positively charged states, and traps that may contain either electrons or holes, producing negative or positive charges, respectively. For simplicity, we consider charge to be a continuous quantity without specific reference to the trapping mechanism. To develop our theoretical framework, we use the Preisach hysteresis model [29, 30], which has been applied to many magnetic systems but has not been widely utilized for electronic hysteresis. The Preisach model approximates hysteretic behavior by representing the response of a system as a collection of hysterons. A hysteron is a generalization of a hysteretic behavior by representing the response of a system to many magnetic systems but has not been widely utilized for electronic hysteresis. The Preisach model approximates hysteretic behavior by representing the response of a system as a collection of hysterons.

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An equilibrium current (Ieq), defined as the average drain current over 100 s after executing the restoring waveform for both the positive and negative gate voltage pulses, was subtracted from the drain current for both measurements. Without any restoring waveform, the current fails to reach equilibrium (Ieq) after 100 s, but with the restoring waveform, both responses after +9 and −9 V gate voltage pulses fall nearly on top of each other and remain near the constant Ieq throughout. This further demonstrates that the restoring waveform D forces charges into a neutral configuration for both large positive and negative gate voltage pulses, and that the charge configuration is stable with time.

$$R_{apf}(V_{gs}) = \begin{cases} 
-1 & \text{for } V_{gs} < \alpha \\
1 & \text{for } V_{gs} > \beta \\
k & \text{for } \alpha < V_{gs} < \beta
\end{cases}$$

where $k$ is the previous $R_{apf}$ value.

In our transistors, $R$ represents the effective gate potential seen by the nanotube as a sum of the influence of the
applied gate potential and the influence of the charge trapped in the gate dielectric. For any given pair of \((\alpha, \beta)\) values, \(R_{gd}\) represents a discrete step-function hysteretic response. A smooth and continuous response may be constructed by defining a hysteron density function, \(\eta(\alpha, \beta)\), and integrating \(R_{gd}\) in the \(\alpha-\beta\) parameter space with \(\eta\) as a weighting function. Thus, any simple first-order hysteretic response can be represented by appropriate choice of the \(\eta(\alpha, \beta)\) density function [29, 30].

To numerically test a restoring waveform that can be applied to any hysteretic SWNT FET, we use a simple numerical model in which \(\eta(\alpha, \beta)\) is chosen to reflect a discrete set of equally spaced hysterons in the \(\alpha-\beta\) parameter space across a square \(\alpha-\beta\) grid, with all hysterons equally weighted. The spacing of this grid is chosen to be 0.2 V. Hysterons with \(\alpha > \beta\) are undefined, representing an unphysical type of hysteresis, and thus we set their weighting to zero. This leaves only half of the \(\alpha-\beta\) plane, defined as \(\alpha < \beta\), corresponding to active hysterons. The gate voltage with the source at ground potential, \(V_{gs}\), can be treated as the input parameter, and the output is the sum of the equally weighted hysterons, computed for each input value. For further simplicity, we truncate the sum of \(\eta(\alpha, \beta)\) within the space of \(|\alpha| < 10 \text{ V}\) and \(|\beta| < 10 \text{ V}\). When \(V_{gs}\) is at its maximum value (+10 V in the numerical simulation described here), all of the \(\beta\) thresholds have been crossed, and all of the hysterons are on (positive). When \(V_{gs}\) is at its minimum value (−10 V), all of the \(\alpha\) thresholds have been crossed, and all of the hysterons are off (negative).

Since every hysteron must be either on or off, the simplest neutral state with \(V_{gs} = 0\) would have half of the hysterons in the on state and half in the off state. The simplest division of the \(\alpha-\beta\) plane in half is along the line \(\alpha = -\beta\), which are the symmetric hysterons with threshold values centered about \(V_{gs} = 0\). Thus, we define the desired hysteron state for charge neutrality as half of the hysterons (\(\alpha < -\beta\)) in the on state and the other half (\(\alpha > -\beta\)) off. Merely sweeping the gate voltage from the maximum value to zero would not produce this state because all of the hysterons with \(\alpha < 0\) would remain on. Similarly, sweeping the gate voltage from the minimum value to zero would leave all the hysterons with \(\beta > 0\) off. In addition, sweeping the gate voltage the entire range from the maximum value to the minimum value would not produce the desired neutral state. One effective method to coerce the hysterons into such a state is to approach \(V_{gs} = 0\) by alternating the input polarity as the input magnitude is decreased. A simple way to describe this method is with the following For–Next algorithm, given as equation (2), where \(N\) is the number of oscillations and \(V_{gs\ max}\) is the maximum input voltage magnitude.

For \(i = 0\) to \(N\)

\[
V_{gs} = V_{gs\ max}\left(1 - \frac{i}{N}\right); \quad \text{wait 1 ms;}
\]

\[
V_{gs} = -V_{gs\ max}\left(1 - \frac{i}{N}\right); \quad \text{wait 1 ms;}
\]

Next \(i\)

Figure 5. Plot of the sum of the relay function \(R_{gd}(V_{gs})\) using the Preisach hysteresis model with evenly spaced, equally weighted hysterons. The full sweep from \(V_{gs} = -10\) to +10 V and back to −10 V is plotted in gray. An alternating input with four oscillations is plotted in black with the red point corresponding to the final value. The inset shows the \(\alpha-\beta\) plane corresponding to the final outcome of the alternating input. Hysterons in the on state (positive) are shown in red while those in the off state (negative) are in black.

To test this restoring waveform, simulations of the Preisach model were conducted using MATLAB. The results are shown in figure 5. Full sweeps made between \(V_{gs} = \pm 10\) V by steps of 0.1 V are shown in gray. As expected with equally weighted hysterons, the hysteresis is centered about \(V_{gs} = 0, V_{\text{effective}} = 0\), the point of our desired neutral hysteron occupation. A restoring waveform with \(N = 4\) is shown in black, with the red dot marking the final value. Each oscillation brings the output closer to the origin, with \(V_{\text{effective}}\) finishing slightly below the neutral point. The inset of figure 5 is the \(\alpha-\beta\) plane corresponding to the hysteron occupations resulting from the \(N = 4\) sweep, where hysterons in black are off and hysterons in red are on. A stair-like division between on and off along the \(\alpha < -\beta\) line is visible. More hysterons are off than on, producing an effective gate potential slightly below 0. By increasing the number of oscillations (\(N\)), the hysterons would become more equally balanced between on and off and the final effective value approaches zero.

For the pulsed waveforms (B, C, and D), variations in the drain current at a given gate voltage are due to the trapped charge population immediately before the gate voltage measurement pulse is executed. One way to evaluate the trapped charge before the measurement pulses is to observe the drain current when the gate is at \(V_{gs} = 0\), between the measurement pulses. These data for the three pulsed waveforms are shown in figure 6(a), along with the expected \(V_{\text{effective}}\) for each waveform from the Preisach model in figure 6(b). The horizontal axes in both figures 6(a) and (b) correspond to the magnitude of the most recent previous gate voltage pulse, and all of the data in figure 6(a) were acquired at
the same experimental conditions ($V_{gs} = 0 \text{ V}, V_{ds} = 5 \text{ V}$). For each waveform, the drain current was recorded 1 ms before the next gate voltage pulse was executed. For waveform B, this corresponds to 10 s after the measurement pulse; for waveform C, it corresponds to 1 ms after the measurement pulse; and for waveform D, it corresponds to 1 ms after the restoring waveform was executed, roughly 70 ms after the measurement pulse.

The data from all three waveforms qualitatively match the forms expected from the Preisach model, even though the Preisach model is not explicitly time-dependent and the hysterons used in the model were all equally weighted, without matching the $I_d$-$V_{gs}$ transistor response curve for the specific device. If all of the charges return to the same configuration between measurements, the drain current at $V_{gs} = 0$ should return to a constant value and a horizontal line would be expected, as shown for sweep D in figure 6(b). However, the data for waveforms B and C reveal a drain current dependence on the previous gate voltage pulse, as expected if charge remains trapped in the dielectric. Furthermore, both waveforms B and C do exhibit hysteresis in this data. This suggests that traps remain occupied from more than one previous measurement pulse. Waveform C decreases this effect by alternating the polarity of the measurement pulses, but there remains a dependence upon the measurement history that is captured within the Preisach model. In contrast, the drain current acquired at $V_{gs} = 0$, between measurements with waveform D, shows no visible hysteresis and only a slight dependence on the previous gate voltage pulse for large values of $V_{gs}$ Pulse. The lack of hysteresis in these data corresponds to the lack of hysteresis in the transfer curve shown in figure 3. The lack of dependence on the previous measurement pulse indicates that the trapped charge is being neutralized between measurements, as intended.

The Preisach model clearly demonstrates its predictive power for the outcome of different measurement protocols in the presence of hysteretic response. It may be desirable for more advanced modeling to track the actual physical location of the trapped charge during the restoring waveform. While this is outside of the scope of the present study, a recent publication supports this model with real-space experimental observations of SiO$_2$ charging around a single SWNT FET using electrostatic force microscopy (EFM) [31]. This study shows that charges of opposite sign can be injected into the gate dielectric with a spatial range that is determined by the magnitude of $V_{gs}$. This suggests that our protocol achieves charge neutrality by injecting closely spaced regions with charge of opposite signs that only need to diffuse a small distance locally to achieve a quasi-neutral configuration.

6. Conclusion

We have presented a measurement technique capable of minimizing the effects of trapped charges in encapsulated SWNT FETs. The gate voltage waveform used is optimized within the Preisach hysteresis model to use the gate electric field to force charges into a quasi-neutral configuration. When used to acquire a transfer curve, this waveform effectively eliminates the hysteresis, and a full transfer curve can be taken in less than one minute using measurement equipment with 1 ms time resolution. The restoration of the same neutral charge configuration after each measurement pulse is verified.
by the consistent drain current value at $V_{gs} = 0$ between measurement pulses. The stability of the neutral charge configuration is verified by the lack of time dependence in the drain current after large measurement pulses, which is shown to be significant without the restoration technique. The ability to quickly set a stable and reproducible charge configuration should allow for the extraction of accurate physical parameters from otherwise history-dependent SWNT devices.

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