A Compact Variable-Temperature Broadband Series-Resistor Calibration

Nathan D. Orloff, Jordi Mateu, *Member, IEEE*, Arkadiusz Lewandowski, *Member, IEEE*, Eduard Rocas, *Student Member, IEEE*, Josh King, Dazhen Gu, *Member, IEEE*, Xiaoli Lu, Carlos Collado, *Member, IEEE*, Ichiro Takeuchi, and James C. Booth

***Abstract*—We present a broadband on-wafer calibration from 45 MHz to 40 GHz for variable temperature measurements, which requires three standards: a thru, reflect, and series resistor. At room temperature, the maximum error of this technique, compared to a benchmark nine-standard multiline thru-reflect-line (TRL) method, is comparable to the repeatability of the benchmark calibration. The series-resistor standard is modeled as a lumped-element π-network, which is described by four frequency-independent parameters. We show that the model is stable over three weeks, and compare the calibration to the multiline TRL method as a function of time. The approach is then demonstrated at variable temperature, where the model parameters are extracted at 300 K and at variable temperatures down to 20 K, in order to determine their temperature dependence. The resulting technique, valid over the temperature range from 300 to 20 K, reduced the total footprint of the calibration standards by a factor of 17 and the measurement time by a factor of 3.**

***Index Terms*—Calibration, cryogenic, error correction, microwave, scattering parameters, series resistor, temperature.**

I. Introduction

MEASUREMENT-BASED circuit modeling of devices is an important design tool for the development of microwave components and systems. Since typical measurement and test systems possess their own frequency-dependent response, accurate modeling and characterization of devices over a broad range of frequencies is challenging without effective correction techniques. A variety of calibration techniques have been developed to address this issue, and are routinely applied to coaxial and on-wafer measurements. Among them, multiline thru-reflect-line (TRL) [1], [2] is considered to be one of the most accurate because of its basis in circuit theory, and is often used as a benchmark for new calibrations [3], [4]. Apart from the multiline TRL technique, Padmanabhan *et al.* [5] recently showed that on-wafer open-short-load-thru (OSLT) calibrations can have comparable accuracy to the multiline TRL approach provided that the shunt-resistor loads are adequately modeled to account for their high-frequency response. Moreover, the development of a compact OSLT calibration greatly reduced the footprint and total measurement time needed to accurately correct room temperature broadband measurements to 110 GHz.

Temperature-dependent experiments are ubiquitous in scientific literature as they often elucidate fundamental thermodynamics and temperature-dependent properties of materials, including conductors and dielectrics. For cryogenic experiments, the relatively large number of standards needed to correct broadband microwave measurements by the multiline TRL method, as compared to OSLT, implies longer measurement times and limits the number of measurements that can be achieved in a single cool-down. Above room temperature, there are also instances where we must limit the period during which the sample and measurement system are exposed to heat, an example of which would be protein measurements [6]. There are many applications of accurate on-wafer calibrations at temperatures other than room temperature, including materials science engineering applications for thin films [7], characterization biological fluids [8], and cryogenic characterization of various components for communications applications [9], [10]. Designing calibration standards with predictable temperature dependent properties will help reduce measurement time, while also reducing the footprint of the calibration standards, for variable temperature applications.

We have chosen the series-resistor calibration [11] to achieve our goal of designing a standard with a predictable temperature dependence because it requires one less standard than an OSLT, which further decreases the footprint of the calibration devices on the wafer. In addition to the series-resistor standard, the calibration technique employed here also uses a thru and a symmetric short-circuit reflect. Experiments have also shown that the accuracy of the series-resistor calibration can be comparable to the repeatability of multiline TRL [11] at room temperature.

In what follows, we first describe our fabrication procedure for the series-resistor standard, which is a resistive strip embedded in the center conductor of a coplanar waveguide (CPW) [12] [see Fig. 1(a)]. We explain how to use the series resistor to extract the characteristic impedance of the CPW

Manuscript received April 28, 2010; revised September 21, 2010; accepted October 04, 2010. Date of publication December 10, 2010; date of current version January 12, 2011. This work was supported by the National Science Foundation (NSF) under Grant DMR-0520471 (MRSEC) and Grant ARO W911NF-07-1-0410.

N. D. Orloff and I. Takeuchi are with the Department of Physics and the Department of Materials Science and Engineering, University of Maryland at College Park, College Park, MD 20742 USA (e-mail: nathan.orloff@gmail.com; takeuchi@umd.edu).

J. Mateu, E. Rocas, and C. Collado are with the Centre Tecnològic de Telecomunicacions de Catalunya, Universitat Politecnica de Catalunya, Barcelona 08860, Spain (e-mail: jmateu@tsc.ups.edu; eduard.rocas@gmail.com; collado@tsc.ups.edu).

A. Lewandowski, D. Gu, X. Lu, and J. C. Booth are with the National Institute of Standards and Technology, Boulder, CO 80305 USA (e-mail: areklew@nist.gov; dazhen.gu@nist.gov; xiaoli.lu@nist.gov; booth@nist.gov).

J. King is with the Business Department, University of Colorado at Boulder, Boulder, CO 80302 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2010.2091200

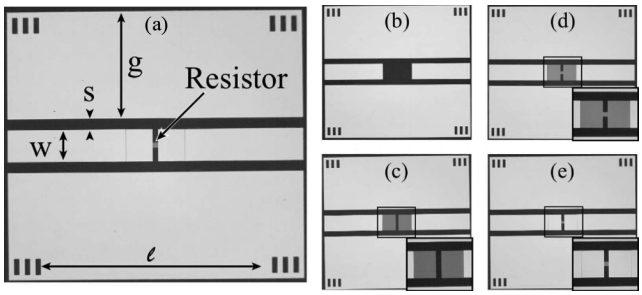

Fig. 1. (a) Representative $Pd_{0.53}Au_{0.47}$ series-resistor standard. The resistive strip is embedded in a gold CPW with a ground plane of width (g), center conductor of width (w), gap of width (s), and resistive strip. The three hash marks on each ground plane are alignment marks for the ground–signal–ground probes. (b) Base electrode layer is fabricated by depositing a 20-nm titanium adhesion layer followed by 330 nm of gold. (c) 1-nm titanium seed layer is used to improve adhesion of the $Pd_{0.53}Au_{0.47}$ pads. (d) 8.5 nm of $Pd_{0.53}Au_{0.47}$ are deposited for the resistor layer. The resistor layer consists of a 10 μm (width) $\times 10$ μm (length) strip which is connected on either side to two large pads, 100 μm $\times$ 50 μm. (e) Electrode layer is electrically connected to the resistor by a 50-nm-thick gold counter electrode layer. The result is a 10 μm $\times$ 10 μm strip embedded in the center of a CPW that is the same length on either side as half the thru standard.

in which it is embedded, and compare it to the characteristic impedance obtained from a more common technique using a shunt resistor. We next describe the modeling procedure used to fit the measured complex S-parameters of the series resistor, which enables us to use it as a calibration standard. We subsequently compare a series-resistor calibration with a multiline TRL calibration at room temperature, and show that the worst case deviations between the two calibrations are comparable to the repeatability error of the multiline TRL calibration. We then demonstrate that the lumped-element circuit parameters used to describe the series resistor are stable over three weeks, and develop a description of the temperature dependence of the lumped-element circuit parameters down to 20 K. We compare the series-resistor calibrations based on a model using parameters with a simplified temperature dependence to series-resistor calibrations where the model is extracted at each measurement temperature and show that this error is also comparable to the repeatability of the benchmark calibration.

II. Fabrication

The series-resistor artifact is the central feature of this calibration technique. The choice of metals used along with the dimensions of the resistive strip make it useful for a broad range of frequencies and affects the temperature dependence of its response. Fig. 1(a) shows a representative 10 μm $\times$ 10 μm series-resistor standard embedded at the center of a gold CPW of length $\ell = 0.43$ mm. The gold CPW has a 100 μm wide center conductor (w), a 10 μm wide gap (s), and 250 μm wide ground planes (g) fabricated on a 0.5-mm-thick low-loss polycrystalline quartz substrate. The composition of the $Pd_{0.53}Au_{0.47}$ resistive strip was inferred from the composition of the target. We chose $Pd_{0.53}Au_{0.47}$ alloy as the resistive material because it has a weak linear temperature dependence from 4 to 500 K [13]. We patterned the devices with conventional photo-lithographic techniques and deposited the metal layers with electron-beam evaporation.

In Fig. 1(b), we show the base electrode layer. We patterned this layer with approximately 1 μm thick lift-off-resist, overcoated using 1 μm thick image resist. The lift-off-resist process ensures well-defined devices and edges for thick conductors [14]. We used electron-beam evaporation to deposit a 20-nm titanium adhesion layer, followed by 330 nm of gold. The remaining layers are sequentially patterned with only 1-μm image resist for each layer. Before depositing each layer in Fig. 1, we use an Argon plasma to clean the surface, which helps to ensure clean metal–metal interfaces.

For the resistor layer, a 1-nm titanium layer [see Fig. 1(c)] is deposited and defines the 100-μm-wide by 50-μm-long pads to promote the adhesion of the resistor and counter-electrode layers. The 8.5-nm-thick $Pd_{0.53}Au_{0.47}$ resistor layer shown in Fig. 1(d), includes the 10 μm $\times$ 10 μm resistive strip and the 100-μm wide by 50-μm-long contact pads. The resistor layer is electrically connected to the electrode layer by depositing 50 nm of gold over the conductors and pads in Fig. 1(e). The entire fabrication process for the series resistor (also used to fabricate separate shunt resistors) presented here required four total deposition layers.

In addition to the series-resistor standard, we also fabricated the devices to complete the benchmark multiline TRL calibration in the base electrode layer. These nine devices included a set of seven CPWs with lengths of $\ell = (0.420\,\text{mm}, 1.000\,\text{mm}, 2.155\,\text{mm}, 3.135\,\text{mm}, 4.200\,\text{mm}, 7.615\,\text{mm}, 11.570\,\text{mm})$, a symmetric short circuit reflect standard, and the series-resistor standard. The reflect standard consisted of a 0.210-mm-long transmission line on each port centered about the termination. For all of the following measurements, we calibrated the network analyzer first with a first-tier coaxial OSLT calibration with a six-position sliding load. We found that this improved the accuracy of the low-frequency response of the on-wafer calibrations and it removed the requirement to directly measure the reflection coefficients of the loads internal to the vector-network analyzer.

III. Determination of the CPW Reference Impedance

Before we can develop the series-resistor calibration, we need to determine the characteristic impedance of the CPW devices that are used in the benchmark multiline TRL calibration. This is typically done using a set of shunt resistors; however, we show that a single series resistor can be used to acquire the same information.

The ability to transform the calibration reference impedance from the characteristic impedance of the CPW to a known reference impedance is valuable for simplifying the modeling of a given device. It is also necessary to transform the reference impedance of the calibration to a real value to compare different calibrations because $|S_{ij}| \leq 1$ is required to achieve quantitative comparison of different calibrations [4]. In the case of the multiline TRL, the calibration is relative to the characteristic impedance of the transmission line (Z_o), which is neither real, nor constant as a function of frequency for normal metal transmission lines. Hence, multiline TRL calibrations need to be transformed to a known reference impedance for calibration comparison.

Williams and Marks [15] showed that a shunt load could be used to approximate Z_o for transmission lines fabricated on low-loss substrates. We can also develop a similar approach using the series resistor, where we make the same assumptions as in [15]. One assumption is that at low frequencies, the impedance of the resistive load (Z_L) can be approximated by dc resistance of the strip $Z_L \approx R_{\rm DC}$. The dc resistance of the strip is determined experimentally from the difference between two-port dc measurements of the series resistor and the thru. For low-loss substrates, such as that employed here, we can assume $G \approx 0$ and $C(\omega) = C_o$, where C_o and G are the capacitance and conductance per unit length of the CPW transmission lines and are constant as a function of frequency. Thus, the characteristic impedance for transmission lines on a low-loss substrate can be simplified as $Z_o \approx \gamma(\omega)/i\omega C_o$, where $\gamma(\omega)$ is the complex propagation constant. We can obtain $\gamma(\omega)$ by either analyzing the corrected S-parameters of a transmission line of known length or from the multiline TRL method. We can later use $\gamma(\omega)$ to translate the reference planes of the resulting calibration.

For the shunt-resistor standard discussed in [5] and [15], the device has two resistive strips, one on port 1 and the other on port 2. In this case, both shunt resistors are needed for the two-port OSLT calibration, otherwise the wafer must be rotated a full 180° so that the device can be measured at both ports. An added benefit of the series-resistor approach is that instead of one reflection coefficient corresponding to a single standard (as is the case for the shunt resistor), all four S-parameters of the series resistor can be used to extract the capacitance per unit length from a measurement of a single resistive strip.

To obtain an estimate for the C_o of the CPW from the series resistor, we start with the simple model for the S-parameters of a series load

$$\mathbf{S} \approx \frac{1}{1+\frac{Z_L}{2Z_o}} \begin{pmatrix} \frac{Z_L}{2Z_o} & 1 \\ 1 & \frac{Z_L}{2Z_o} \end{pmatrix} \tag{1}$$

and make the same definitions and approximations as before. Inserting $Z_o \approx \gamma(\omega)/i\omega C_o$ into (1) and $Z_L \approx R_{\rm DC}$, we can then solve for C_o

$$C_{11,22} \approx \left(\frac{2\gamma(\omega)}{i\omega R_{\rm DC}}\right) \frac{S_{11,22}}{1-S_{11,22}} \tag{2}$$

$$C_{12,21} \approx \left(\frac{2\gamma(\omega)}{i\omega R_{\rm DC}}\right) \frac{1-S_{12,21}}{S_{12,21}}. \tag{3}$$

Once we obtain (2) and (3) from the reflection and transmission coefficients of a single series resistor, we determine C_o by taking the low-frequency limit, which yields for estimates of C_o. Note that (2) and (3) are derived using an oversimplified model of the frequency dependence for the series resistor, where we assume that, at low frequency, $Z_L \approx R_{\rm DC}$.

We demonstrated that the C_o obtained by the series and shunt approaches are equivalent by fabricating both shunt and series-resistor standards in identical CPW transmission lines on polycrystalline quartz substrates. The devices were corrected with multiline TRL calibrations relative to the CPW characteristic impedance $Z_o(\omega)$. We then used (2) and (3) for the series resistor and a similar equation for the shunt resistors [15] to evaluate C_o with $\gamma(\omega)$ determined by the multiline TRL algorithm. Fig. 2 shows C_o as calculated from the two approaches. In Fig. 2, the C_o extracted from the shunt resistors, one on each port, are shown as the solid green (in online version) and black lines. The C_o value extracted from (2) using the reflection coefficient data for series resistor, averaged together, is shown as the solid red line; the corresponding value calculated from (3) using the transmission coefficient data, averaged together, is shown as the solid blue line (in online version). We then use the median value below 1 GHz of $C_o(\omega)$ to estimate C_o at zero frquency and obtain a value of 1.05 pF/cm. This value is consistent with the capacitance per unit length obtained from finite-element simulations of the cross-sectional geometry of these CPW transmission lines on quartz. We can then obtain the reference impedance of the CPW from the expression $Z_o(\omega) \approx \gamma(\omega)/i\omega C_o$. Once we have obtained $Z_o(\omega)$, we can transform the reference impedance to 50 Ω.

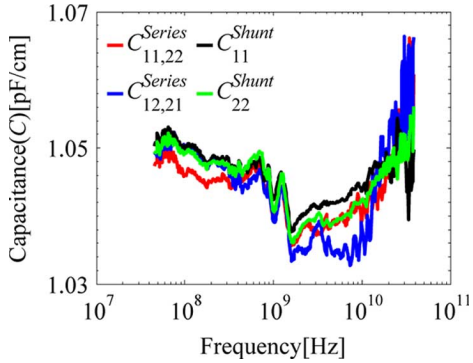

Fig. 2. Comparison of the effective capacitance per unit length extracted from the series-resistor and shunt resistor standards. The red curve (in online version) shows the $C^{\rm Series}_{11,22}$ extracted from the series-resistor transmission coefficients of the corrected S-parameters, and the blue line (in online version) shows the $C^{\rm Series}_{12,21}$ from the reflection coefficients. The black line is $C^{\rm Shunt}_{11}$ extracted from the shunt resistor on port 1, and green (in online version) $(C^{\rm Shunt}_{22})$ for port 2. C_o is determined by taking the low-frequency limit of $C^{\rm Shunt}_{11}$, $C^{\rm Shunt}_{22}$, $C^{\rm Series}_{11,22}$, and $C^{\rm Series}_{12,21}$.

IV. Modeling the Series Resistor

In Section IV, we used the approximation that $Z_L \approx R_{\rm DC}$ to estimate the C_o of the CPW transmission line from measurements of the series resistor, but we need a more accurate model of $Z_L(\omega)$ to use the series resistor as a calibration standard at high frequencies. As a first step toward obtaining a better model of the series resistor, we correct a measurement of the series resistor with multiline TRL calibration (making use of the technique from the previous section to transform to a reference impedance of 50 Ω) with the calibration reference planes translated to either end of the resistive strip using the $\gamma(\omega)$ obtained from the multiline TRL algorithm.

We then transform these corrected S-parameters of the series resistor to an admittance matrix, which we model by a π-network. The series-admittance term describes the response of the resistive strip, and we parameterize this by the resistance (R_s), inductance (L_s), and capacitance (C_s), which are assumed to be frequency independent. In general, there is a shunt admittance $(Y_g = i\omega C_g)$ between the strip and ground plane of the transmission line; however, for these experiments, we found that

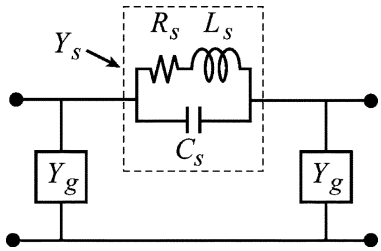

Fig. 3. Equivalent lumped-element circuit model for the series-resistor standard. The series components of the circuit include the resistance (R_s), inductance (L_s), and capacitance (C_s). The shunt element is $Y_g = i\omega C_g$, where C_g is the capacitance to ground.

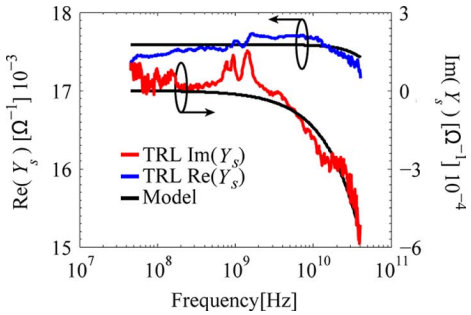

Fig. 4. Comparison of the real part (blue in online proofs) and imaginary part (red in online proofs) of the admittance, Y_s, of the series-resistor standard corrected with the multiline TRL calibration. The modeled Y_s (black) was calculated with the series resistor lumped element model parameters of $R_s = 56.86\ \Omega$, $L_s = 21.90$ pH, and $C_s = 4.52$ fF.

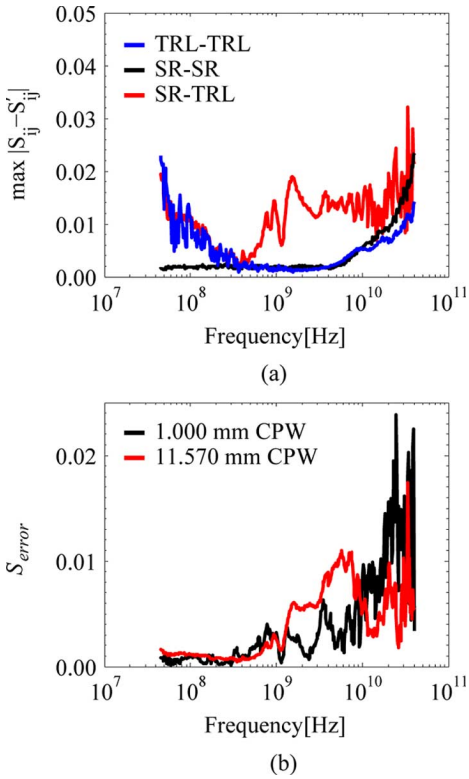

Fig. 5. (a) Maximum error in S-parameters between two successive multiline TRL calibrations is shown as the blue line (in online version) (TRL-TRL). The black line shows the maximum error for two successive calibrations with the series-resistor standard (SR-SR). In red (in online version), we show the maximum error between the series-resistor calibration and multiline TRL (SR-TRL). (b) Difference, S_{error}, in S-parameters for CPWs 1.000- and 11.570-mm-long corrected with multiline TRL and with the series-resistor calibration.

including this term did not affect the overall error. Fig. 3 shows the lumped-element model of the series resistor, with the shunt admittance, Y_g, and the series admittance, Y_s, where

$$Y_s = i\omega C_s + \frac{1}{R_s + i\omega L_s}. \tag{4}$$

We then obtain initial values for R_s, L_s, and C_s in the following manner. A series capacitor, which is identical to the series resistor, except that it has no resistive strip, is used to obtain an estimate for C_s. Using (4) and this value for C_s, we estimated L_s with a linear fit as a function of frequency. R_s was approximated by the dc resistance. We construct the modeled S-parameters using these estimates for R_s, L_s, and C_s. We then minimized the difference between the modeled and measured S-parameters (summed over all frequencies) by varying R_s, L_s, and C_s using the Levenburg–Marquadt algorithm [16]. We define the error to be $S_{\text{error}} = \sqrt{\sum_{i,j=1}^{N=2} |S_{ij}^{\text{TRL}} - S_{ij}^{\text{model}}|^2}$, where S_{ij}^{TRL} are the S-parameters of the series resistor corrected with multiline TRL and S_{ij}^{model} are the S-parameters of the model calculated with the parameters R_s, L_s, and C_s. In Fig. 4, we show the real part (blue in online version) and imaginary part (red in online version) of the series admittance corrected with multiline TRL calibration along with the resulting lumped-element model (black). For the data shown in Fig. 4, we obtain $R_s = 56.86\ \Omega$, $L_s = 21.90$ pH, and $C_s = 4.52$ fF. In practice, the optimized values differ from our initial estimates by at most approximately 10%. From Fig. 4, it is clear that the series-resistor model captures the basic frequency-dependent response of the series resistor, but it cannot explain the fine features such as the small peak around 1 GHz. At present, it is unclear if this is an artifact in the multiline TRL calibration, series-resistor standard, or measurement system; however, future experiments will address this issue in greater detail.

V. Comparison With Multiline TRL

Once we have adequately modeled the frequency-dependent response of the series resistor, we can use this model to perform a calibration using measurements of the series resistor, thru, and symmetric short-circuit reflect and evaluate the accuracy of the series-resistor calibration relative to the benchmark multiline TRL calibration. For the S-parameters of an arbitrary passive device corrected using two different calibrations relative to the same real-valued reference impedance, a matrix corresponding to the maximum errors in each S-parameter can be calculated by the approach outlined in [3] and [4]. Although the error matrix carries information in all four elements, the worst case maximum error ($\max |S_{ij} - S'_{ij}|$) is often used as the metric for comparing calibrations. We use this metric in what follows to compare calibration techniques, like those shown in Fig. 5.

Fig. 5(a) shows $\max |S_{ij} - S'_{ij}|$ for a series of calibrations comparing the series resistor to subsequent series resistor (black), multiline TRL to subsequent multiline TRL (blue in online version), and multiline TRL to series resistor (red in online version). The maximum error between successive multiline TRL calibrations (blue in online version) shows a gradual

TABLE I
SERIES-RESISTOR CIRCUIT PARAMETERS VARIATION OVER A THREE-WEEK PERIOD

Date	$R_{DC}[\Omega]$	$R_s[\Omega]$	L_s[pH]	C_s[fF]
Week 1	56.69	56.86	21.90	4.52
Week 2	56.63	56.81	26.13	4.05
Week 3	56.63	56.83	25.79	4.04

increase below 500 MHz and above 4 GHz. The TRL–TRL maximum error demonstrates the repeatability of the benchmark calibration. The successive series-resistor calibrations (SR-SR) show similar repeatability at high frequencies to the multiline TRL calibration, and show that good repeatability is maintained for very low frequencies. We have also compared the series resistor to TRL (red in online version), which is larger than the repeatability between the successive multiline TRL and successive series-resistor calibrations. At low frequencies, the increase in the maximum error follows the repeatability of the TRL calibration. comparable to the maximum error at high frequency in the repeatability of both calibration techniques and the maximum error is below 2% for the majority of the frequency regime. The measured error in the S-parameters, S_{error}, is shown in Fig. 5(b) for specific devices (CPW of lengths 1.000 and 11.570 mm) where we compute S_{error}, as defined in the previous section, but we take the difference between the measurements corrected with the multiline TRL calibration and the measurements corrected with the series-resistor calibration.

We demonstrated the stability of this technique by repeating both the series resistor and benchmark multiline TRL calibrations each week for a three-week period. In Table I, we report the parameters R_s, L_s, and C_s from Fig. 3 extracted over a three-week period. The R_{DC} values are comparable to the extracted R_s to within 1%. The other circuit parameters showed increased variation from measurement to measurement, but represent a small contribution to frequency-dependent impedance of the series resistor. In Fig. 6(a), we compare the series-resistor calibration to a subsequent multiline TRL calibration using the model parameters extracted on Week 1 over a period of three weeks (Week 1, Week 2, Week 3). Fig. 6(a) shows that the lumped element circuit parameters used to describe the series resistor are stable over relatively long times. In Fig. 6(b), we show the maximum error between series-resistor calibrations using the model from Week 1 and the models extracted on Week 2 and Week 3. The long-term stability of the circuit parameters used to characterize the series resistor is an important issue. Within the conditions of our experiments, we have seen no evidence of degradation in the device response and variation in modelling parameters over a period of approximately one year.

VI. VARIABLE TEMPERATURE

In order to quantify the applicability of the series-resistor calibration over variable temperature, we repeated the analysis described in Section V for measurements at different temperatures, from room temperature down to 20 K. We then examined the temperature-dependent behavior of R_s, L_s, and C_s. We have performed our temperature-dependent measurements with a cryogenic probe station, which maintains the measurement devices and microwave probes under vacuum. The substrate is

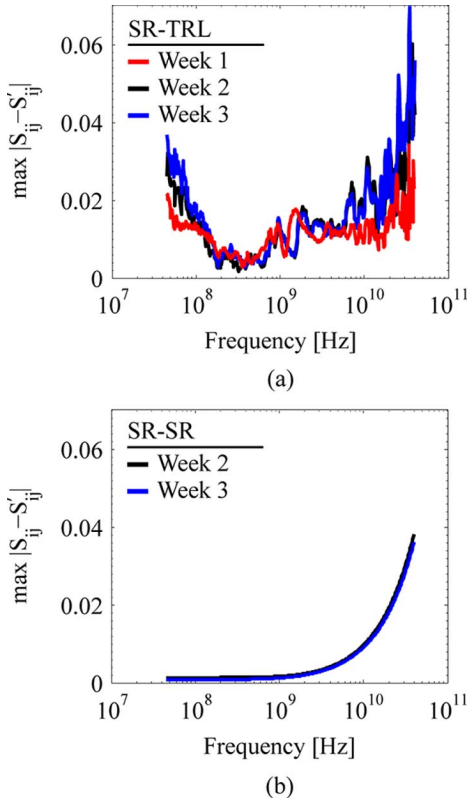

Fig. 6. (a) Maximum error between the series-resistor calibration and the multiline TRL calibration, using the same series-resistor model. Each series resistor calibration was calculated using the model from Week 1. The lumped-element circuit parameters for the series resistor are $R_s = 56.94\ \Omega$, $L_s = 21.90$ pH, and $C_s = 4.55$ fF. The red (in online version), black, and blue (in online version) lines correspond to Week 1, Week 2, and Week 3, respectively. (b) Maximum error between series-resistor calibrations extracted on Week 2 and Week 3 compared to calibrations using the model extracted on Week 1.

TABLE II
SERIES-RESISTOR CIRCUIT PARAMETERS AT VARYING TEMPERATURE

T [K]	$R_{DC}[\Omega]$	$R_s[\Omega]$	L_s[pH]	C_s[fF]
20	51.36	51.57	21.30	1.22
60	51.80	52.09	27.11	2.55
100	53.11	53.42	20.61	2.10
140	53.96	54.18	20.46	2.96
180	54.53	54.84	19.94	3.14
220	55.28	55.56	18.66	2.67
260	56.08	56.26	18.59	3.78
300	56.72	57.03	20.17	2.43

physically, electrically, and thermally connected to a platform with integrated heaters and thermometers that is cooled with a cold finger, which allows us to control the sample and probe temperatures to within ±0.01 K. At each temperature, we performed the benchmark multiline TRL calibration described in Section I and then measured the series-resistor standard.

Table II summarizes the model parameters R_s, L_s, and C_s fit to the data corrected with the multiline TRL calibration at each temperature (as described in Section IV). The capacitance per unit length of the CPW, C_o, was 1.05 pF/cm, and varied by less that 1% as a function of temperature from 300 down to 20 K. Fig. 7 shows the R_s values extracted from the series resistor

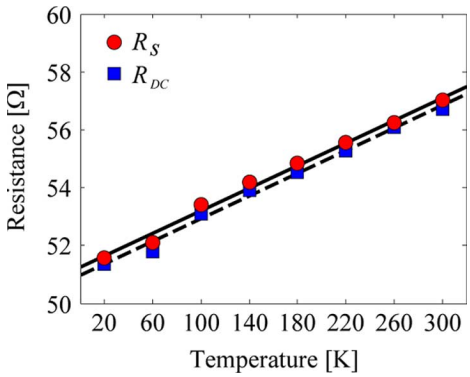

Fig. 7. Temperature dependence of R_s lumped-element circuit parameter of the series-resistor standard, which has been extracted at each temperature with measurements corrected with the multiline TRL calibration. R_s and $R_{\rm DC}$ are shown as discrete red circles and blue (in online version) squares, respectively. R_s is fit by the solid black line and $R_{\rm DC}$ is fit by the dashed black line. The equation for the solid black line is $R_s(\mathrm{T}) = 51.27\ \Omega + 0.02[\Omega \cdot \mathrm{K}^{-1}] \cdot \mathrm{T}$ and the dashed black line is $R_{\rm DC}(\mathrm{T}) = 50.98\ \Omega + 0.02[\Omega \cdot \mathrm{K}^{-1}] \cdot \mathrm{T}$.

over the measured temperature range. The R_s extracted from the series resistor can be linearly fit as a function of temperature by $R_s(\mathrm{T}) = 51.27\,\Omega{+}0.02[\Omega{\cdot}\mathrm{K}^{-1}]{\cdot}\mathrm{T}$. The dashed black line in Fig. 7 is the fit to the dc resistance, $R_{\rm DC}(\mathrm{T}) = 50.98\,\Omega{+}0.02[\Omega{\cdot}\mathrm{K}^{-1}] \cdot \mathrm{T}$. L_s and C_s showed comparatively weak temperature dependence. Varying L_s and C_s away from the value extracted at 300 K did not significantly affect the magnitude or frequency dependence of the maximum error.

Given the small changes in the model parameters as a function of temperature, we explored the possible use of the room-temperature model parameters to correct low-temperature measurement data. The dashed lines in Fig. 8(a) are the maximum error between a series-resistor calibration using the 300-K model and one where the model parameters are extracted at the given temperature. For clarity, we show only 20 K (red in online version), 100 K (blue in online version), and 180 K (black) data sets in Fig. 8(a). This figure shows, as expected, that significant errors are generated by applying a room-temperature series-resistor calibration to data measured at lower temperatures.

To improve the accuracy of the low-temperature calibration without extracting the series-resistor model at each individual temperature, we can fit the temperature dependence of the model parameters, such as $R_s(\mathrm{T})$. In Fig. 8(a), the solid lines show the maximum error between a series-resistor calibration at the given temperature and one where the linear fit used is to calculate $R_s(\mathrm{T})$, while L_s and C_s values from the 300 K are used. Fig. 8(b) shows the solid lines from Fig. 8(a) in greater detail. The solid gray line in Fig. 8(b) is the maximum error between the modeled temperature dependence of $R_s(\mathrm{T})$ evaluated at 300 K and model extracted at 300 K. The solid gray line illustrates the effect of only changing R_s, and therefore, has no frequency dependence because L_s and C_s are the same as those extracted at 300 K without extracting the model at each temperature.

Fig. 8 demonstrates that by simply allowing for temperature dependence of $R_s(\mathrm{T})$ we can dramatically reduce the maximum error for any temperature between 300–20 K. We also calculated the maximum error at each temperature between the series

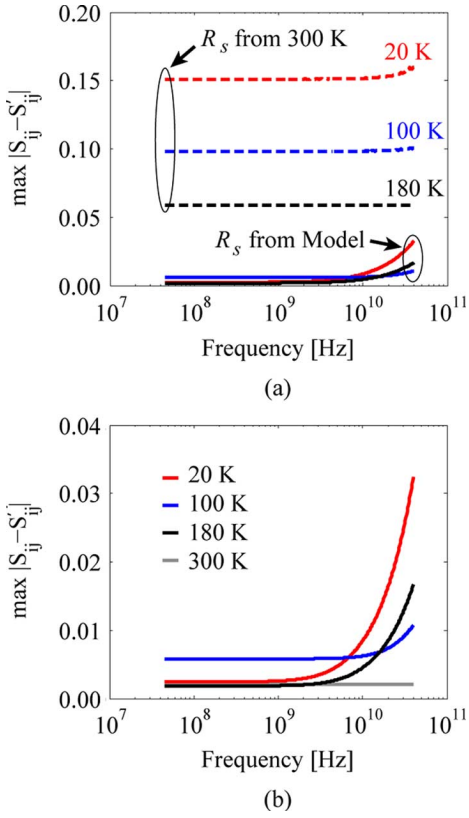

Fig. 8. (a) Dashed lines compare a series-resistor calibration using the model extracted at 300 K compared to a calibration using the model extracted at 20 K (red in online version), 180 K (blue in online version), and 300 K (black). The model extracted at each temperature was calibrated with a multiline TRL calibration conducted at that temperature. The solid lines show the maximum error between to series-resistor calibrations using the model extracted at a given temperature compared to one using the temperature dependent model for $R_s(\mathrm{T})$ and the 300-K values for L_s and C_s. (b) Solid lines from (a) are shown in more detail with the maximum error for the 300-K calibration in light gray using the predicted temperature dependence of $R_s(\mathrm{T})$ and the actual extracted value.

resistor and multiline TRL calibrations and found it to be similar in magnitude and frequency dependence to that shown in Fig. 5(a).

We can apply these results to create a compact calibration set for use from 45 MHz to 40 GHz at variable stable temperatures. Our compact variable-temperature calibration set includes a series resistor, thru, and symmetric short circuit reflect. The series resistor can be modeled after an initial characterization at room temperature that includes a correction with a brenchmark multiline TRL calibration. Once the series resistor is characterized at room temperature, dc measurements of the series resistance as a function of temperature can be used to obtain $R_s(\mathrm{T})$, and the compact series-resistor calibration can be applied at variable static temperatures to correct broadband microwave measurements. Also, based on the frequency response of the series resistor, this technique can be extended to lower frequencies, where it is similar to the line-reflect-match technique [17].

VII. Conclusion

We have demonstrated a broadband on-wafer calibration technique based on a series-resistor artifact that decreased the total area required for the calibration standards by a factor of 17 compared to a nine-standard multiline TRL calibration.

By parameterizing the response of the series resistor with a simple model, we obtained a maximum error comparable to the repeatability of the benchmark multiline TRL calibration for room temperature calibrations. We showed that the parameters extracted using this simple model were relatively stable over a period of three weeks. We also found that the series-resistor calibration showed improved repeatability compared to a nine standard multiline TRL calibration at frequencies below 1 GHz, and the technique can easily be extended to even lower frequencies. In addition to greatly reducing the footprint and measurement time, the series resistor could also be used to extract the characteristic impedance of transmission lines on low-loss substrates. We demonstrated that the predictable temperature response of the series-resistor artifact enabled compact broadband on-wafer calibrations that can be applied over a wide range of temperatures with a minimal increase in maximum error.

ACKNOWLEDGMENT

The authors thank Y. Wang, National Institute of Standards and Technology (NIST), Boulder, CO, T. M. Wallis, NIST, D. F. Williams, NIST, U. Arz, Physikalisch-Technische Bundesanstalt, Braunschweig, Germany, and D. K. Walker, NIST, for their critical review of this paper's manuscript and valuable contributions to this work. The authors also thank D. LeGovlan, NIST, for his help in performing the coaxial OSLT calibrations.

REFERENCES

[1] R. B. Marks, "A multiline method of network analyzer calibration," *IEEE Trans. Microw. Theory Tech.*, vol. 39, no. 7, pp. 1205–1215, Jul. 1991.

[2] D. F. Williams, J. C. M. Wang, and U. Arz, "An optimal vector-network-analyzer calibration algorithm," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 12, pp. 2391–2401, Dec. 2003.

[3] D. F. Williams, R. B. Marks, and A. Davidson, "Comparison of on-wafer calibrations," in *Proc. 38th ARFTG Conf. Dig.–Winter*, Dec. 1991, vol. 20, pp. 68–81.

[4] R. B. Marks, J. A. Jargon, and J. R. Juroshek, "Calibration comparison method for vector network analyzers," in *Proc. 48th ARFTG Conf. Dig. –Fall*, Dec. 1996, vol. 30, pp. 38–45.

[5] S. Padmanabhan, L. Dunleavy, J. E. Daniel, A. Rodriguez, and P. L. Kirby, "Broadband space conservative on-wafer network analyzer calibrations with more complex load and thru models," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 9, pp. 3583–3593, Sep. 2006.

[6] D. Rees and A. Robertson, "Some thermodynamic implications for the thermostability of proteins," *Protein Sci.*, vol. 10, no. 6, pp. 1187–1194, Jun. 2001.

[7] N. Orloff, W. Tian, C. Fennie, C. Lee, D. Gu, J. Mateu, X. Xi, K. Rabe, D. Schlom, I. Takeuchi, and J. Booth, "Broadband Dielectric Spectroscopy of Ruddlesden-Popper $Sr_{n+1}Ti_nO_{3n+1}$ $(n = 1, 2, 3)$ Thin Films," *Appl. Phys. Lett.*, vol. 94, no. 4, Jan. 2009, Art. ID 042908 (3 pp).

[8] J. C. Booth, N. D. Orloff, J. Mateu, M. Janezic, M. Rinehart, and J. A. Beall, "Quantitative permittivity measurements of nanoliter liquid volumes in microfluidic channels to 40 GHz," *IEEE Trans. Instrum. Meas.*, vol. 59, no. 12, pp. 3279–3288, Dec. 2010.

[9] H. Meschede, R. Reuter, J. Albers, J. Kraus, D. Peters, W. Brockerhoff, F.-J. Tegude, M. Bode, J. Schubert, and W. Zander, "On-wafer microwave measurement setup for investigations on HEMTs and high-Tc superconductors at cryogenic temperatures down to 20 K," *IEEE Trans. Microw. Theory Tech.*, vol. 40, no. 12, pp. 2325–2331, Dec. 1992.

[10] J. Laskar, J. J. Bautista, M. Nishimoto, M. Hamai, and R. Lai, "Development of accurate on-wafer, cryogenic characterization techniques," *IEEE Trans. Microw. Theory Tech.*, vol. 44, no. 7, pp. 1178–1183, Jul. 1996.

[11] D. F. Williams and D. K. Walker, "Series-resistor calibration," in *Proc. 50th ARFTG Conf. Dig.–Fall*, Dec. 1997, vol. 32, pp. 131–137.

[12] C. P. Wen, "Coplanar waveguide: A surface strip transmission line suitable for nonreciprocal gyromagnetic device applications," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-17, no. 12, pp. 1087–1090, Dec. 1969.

[13] J. Conybeare, "The resistance of palladium and palladium–gold alloys," *Proc. Phys. Soc.*, vol. 49, pp. 29–37, Jan. 1937.

[14] Y. Chen, K. Peng, and Z. Cui, "A lift-off process for high resolution patterns using PMMA/LOR resist stack," *Microelectron. Eng.*, vol. 73–74, pp. 278–281, 2004.

[15] D. F. Williams and R. B. Marks, "Transmission line capacitance measurement," *IEEE Microw. Guided Wave Lett.*, vol. 1, no. 9, pp. 243–245, Sep. 1991.

[16] D. W. Marquardt, "An algortihm for least-squares estimation of nonlinear paramters," *J. Soc. Indus. Appl. Math.*, vol. 11, no. 2, pp. 431–441, 1963.

[17] D. F. Williams and R. B. Marks, "LRM probe-tip calibrations using nonideal standards," *IEEE Trans. Microw. Theory Tech.*, vol. 43, no. 2, pp. 466–469, Feb. 1995.

Nathan D. Orloff was born in Columbia, SC, on August 10, 1981. He received the B.S. degree in physics (with high honors) from the University of Maryland at College Park, in 2004, and is currently working toward the Ph.D. degree at the University of Maryland at College Park. His doctoral thesis concerns the study and extraction of microwave properties of ferroelectrics and fluids.

Mr. Orloff was the recipient of the 2004 Martin Monroe Undergraduate Research Award, the 2006 CMPS Award for Excellence for Teaching Assistants, and 2010 Michael J. Pelczar Award for Excellence in Graduate Education.

Jordi Mateu (M'03) received the Telecommunication Engineering and Ph.D. degrees from the Universitat Politècnica de Catalunya (UPC), Barcelona, Spain, in 1999 and 2003, respectively.

He is currently an Associate Professor with UPC, and an Associate Researcher with Centre Tecnològic de Telecomunicacions de Catalunya, UPC. In Summer 2001, he was a Visiting Researcher with Superconductor Technologies Inc., Santa Barbara, CA. Since September 2004, he has held several Guest Researcher appointments with the National Institute of Standards and Technology (NIST), Boulder, CO, where he was a Fulbright Research Fellow from 2005 to 2006. From 2003 to 2005, he was a Part-Time Assistant Professor with the Universitat Autonoma de Barcelona.

Arkadiusz Lewandowski (M'09) received the M.Sc. degree in electrical engineering and Ph.D. degree in microwave measurements from the Warsaw University of Technology, Warsaw, Poland, in 2001 and 2009, respectively.

In 2002, he joined the Institute of Electronics Systems, Warsaw University of Technology. Since 2004 he has been a Guest Researcher with the National Institute of Standards and Technology (NIST), Boulder, CO, where he is engaged in the development of uncertainty analysis and calibration methods for coaxial and on-wafer VNA measurements.

Mr. Lewandowski was the recipient of Best Paper Award of the International Microwave Conference MIKON 2008, Wroclaw, Poland, and the 2005 IEEE Microwave Theory and Techniques Society (IEEE MTT-S) Graduate Fellowship Award in 2002.

Eduard Rocas (S'06) was born in Palafrugell, Catalonia, Spain, in 1982. He received the Telecommunication Engineering degree from the Universitat Polit ècnica de Catalunya (UPC), Barcelona, Spain, in 2005, and is currently working toward the Ph.D. degree at the UPC.

Mr. Rocas was the recipient of a Formación del Profesorado Universitario grant and a Formación de Personal Investigador grant.

Josh King was born in Denver, CO, in 1988. He is currently working toward the B.A. degree in business from the University of Colorado at Boulder.

Dazhen Gu (S'01–M'08) received the Ph.D. degree in electrical engineering from the University of Massachusetts–Amherst, in 2007.

Since November 2003, he has been with the Electromagnetics Division, National Institute of Standards and Technology (NIST), Boulder, CO. In May 2007, he joined the Microwave Measurement Services Project, where he has been involved in microwave metrology, in particular thermal noise measurements and instrumentation, and fabrication of on-wafer devices for ultra-wideband material calibration and nanowire characterization.

Xiaoli Lu, photograph and biography not available at time of publication.

Carlos Collado (A'02–M'03) received the Telecommunication Engineering and Ph.D. degrees from the Universitat Politècnica de Catalunya (UPC), Barcelona, Spain, in 1995 and 2001, respectively, and the M.S. degree in biomedical engineering from UPC, in 2002.

In 1998, he joined the faculty of UPC, and he became an Associate Professor in 2005. From 2005 to 2008, he was Vice-Dean of the Technical School of Castelldefels, where he is responsible for tthe telecommunication and aeronautic engineering degrees. He was a Visiting Researcher with the University of California at Irvine in 2004 and with the National Institute of Standard and Technology (NIST) from 2009 to 2010. His primary research interests include microwave devices and systems.

Ichiro Takeuchi received the B.S. degree in physics from the California Institute of Technology, Pasadena, in 1987, and the Ph.D. degree in physics from the University of Maryland at College Park, in 1996.

From 1996 to 1998, he was a Postdoctoral Fellow with the Lawrence Berkeley National Laboratory. Since 1999, he has been on the faculty of the Department of Materials Science and Engineering, University of Maryland at College Park, where he is currently a Professor. His research focuses on the development and applications of the combinatorial approach to electronic and magnetic materials, multilayer thin-film devices, and scanning probe microscopes.

James C. Booth received the B.A. degree in physics from the University of Virginia, Blacksburg, in 1989, and the Ph.D. degree in physics from the University of Maryland at College Park, in 1996.

Since 1996, he has been a Physicist with the National Institute of Standards and Technology (NIST), Boulder, CO, originally as a National Research Council (NRC) Post-Doctoral Research Associate (1996–1998) and currently as a Staff Scientist. His research with NIST is focused on exploring the microwave properties of new electronic materials and devices including ferroelectric, magnetoelectric, and superconducting thin films, as well as developing experimental platforms integrating microfluidic and microelectronic components for RF and microwave frequency characterization of liquid and biological samples.